

P27162.A07  
Serial No.: 10/667,601

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Dureseti CHIDAMBARRAO, *et al.*      Conf. No: 9755  
Group Art Unit: 2812  
Appln. No. : 10/667,601      Examiner: KENNEDY, Jennifer M.  
Filed : September 23, 2003  
For : IMPROVED NFETs USING GATE INDUCED STRESS MODULATION

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
U.S. Patent and Trademark Office  
Customer Service Window, Mail Stop AF  
Randolph Building  
401 Dulany Street  
Alexandria VA 22314

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, and supplemental to the Information Disclosure Statement filed on October 11, 2005, applicant respectfully brings the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application.

Further to the U.S. Patent and Trademark Office's decision to waive the requirement under 37 C.F.R. § 1.98 (a)(2)(i), copies of the U.S. patents and U.S. published patent applications are not enclosed herewith. However, if any copies are needed, the Examiner is respectfully requested to contact the undersigned.

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Applicants respectfully request that the Examiner consider the materials cited and indicate such consideration by appropriately initialing the enclosed PTO-1449 Form and including a copy of the initialed form in the next official communication.

Applicants note that a Petition to Withdraw the Application from issue and a Request for Continued Examination (RCE) have been filed with the Office of Petitions on even date. Therefore, copies these documents are enclosed.

Applicants acknowledge that this Supplemental Information Disclosure Statement (SIDS) is being filed after payment of the issue fee. However, Applicants are concurrently filing this SIDS as a submission to the filing of a Request for Continued Examination (RCE) along with the fee for filing an RCE, and a petition to request withdrawal of the application from issue. Accordingly, Applicant respectfully requests consideration of the above-noted documents.

Should there be any questions concerning this application, the Examiner is invited to contact the undersigned at the below listed telephone number.

Respectfully submitted,  
Dureseti CHIDAMBARRAO, *et al.*



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FORM PTO-1449		U.S. Department of Commerce Patent and Trademark Office		Atty. Docket No. P27162	Application No. 10/667,601		
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use several sheets if necessary)				Applicant Dureseti CHIDAMBARRAO et al.			
				Filing Date September 23, 2003		Group 2812	
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		US 2002/0063292 A1	5-30-2002	Armstrong et al.			
		US 2003/0032261 A1	2-13-2003	Yeh et al.			
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		6,974,981	12-13-2005	Chidambarao et al.			
		6,977,194	12-20-2005	Belyansky et al.			
<b>FOREIGN PATENT DOCUMENTS</b>							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
		JP 64-76755	3-22-1989	Japan			X
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
EXAMINER				DATE CONSIDERED			
*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
		G. Zhang, et al., "A New 'Mixed-Mode' Reliability Degradation Mechanism in Advanced Si and SiGe Bipolar Transistors." IEEE Transactions on Electron Devices, vol. 49, no. 12, December 2002, pp. 2151-56.					
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